Design and Performance of *I*-Band (8–10-GHz) TRAPATT Diodes and Amplifiers

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Abstract—**The design and fabrication of *I*-band silicon TRAPATT diodes are described, and the results of both oscillator and amplifier measurements are presented. The paper includes details of the design and characterization of a cascaded three-stage TRAPATT amplifier.**

I. Introduction

THE HIGH-CONVERSION efficiency of the TRAPATT oscillator or amplifier makes it a contender for the solid-state replacement of TWT's at frequencies as high as 10 GHz. As oscillators, peak powers of 15 W have been demonstrated in *I* band with conversion efficiencies of up to 36 percent and as amplifiers, added-power efficiencies of 25 percent have been obtained. Duty factors as high as 12.5 percent have been realized with mean output powers in excess of 1 W.

This contribution describes circuit and diode design details and the characteristics of a three-stage TRAPATT amplifier operating at 9.6 GHz. The amplifier operates in a class-C mode, dissipating power solely during the pulse period, thereby maintaining peak efficiency from high duty factors to single-shot operation.

II. Device Design and Fabrication

Practical realization of *I*-band TRAPATT diodes requires careful consideration of many aspects of device production. The inpurity doping profile of the semiconductor material from which diodes are to be fabricated must be accurately controlled. Diode design and the method of fabrication must be directed towards producing a structure which provides efficient removal of heat from the device, and the devices ideally should be bonded into a package, the electrical and thermal properties of which impose minimal constraints upon the performance of the diode/circuit combination.

A. Material Growth and Characterization

The impurity doping profile of a conventional p^+-n-n^+ TRAPATT diode consists of a narrow n-type active region with abrupt p^+-n and n-n^+ interfaces. Under avalanche breakdown of the p^+-n junction, this structure is heavily punchthrough, the punchthrough factor F being defined by

$$F=\sqrt{\left(\frac{V_B}{V_P}\right)}$$

where V_B is the breakdown voltage of a nonpunchthrough diode with the same doping level and V_P is the punchthrough voltage.

The value of F for a practical TRAPATT diode is typically as high as six. It has been found, in practice, that devices with abrupt p^+-n junctions are prone to burn out at low input power levels, whereas those fabricated from material with a graded p^+-n region are able to operate reliably at current densities commensurate with high efficiencies. The n-n^+ interface, however, is designed to be as abrupt as possible in order to reduce parasitic loss under large-signal modulation.

Low-resistivity arsenic-doped substrates minimize the device parasitic resistance and produce a low-resistance ohmic contact. The high solubility of arsenic in silicon which is achievable ($\approx 5\times 10^{19}$ atoms/cm^3) enables resistivities as low as 0.0015 $\Omega\cdot$cm to be realized. However, as arsenic is highly volatile, measures must be taken to contain it during any exposure of the silicon to high temperatures. The n-layer is grown by vapor phase epitaxy by the pyrolysis of silane. This method combines a high degree of doping and thickness control with a relatively low temperature (1075°C), thus minimizing n-n^+ interface degradation during growth. Prior to growth, a coating of silicon dioxide is grown at high temperature in steam to completely cover the substrate. Phosphorus-doped silicon is epitaxially grown onto the substrate through a window etched in the oxide. The oxide prevents the escape of arsenic from the substrate surfaces which would contribute to the n-layer doping in an uncontrollable manner.

Characterization of the n-layer doping level is achieved using a J.A.C. automatic profiler [1] in conjunction with a mercury Schottky-barrier diode on the surface of the grown layer. As the width of the n-type active region of the TRAPATT structure is critical and represents only about one-seventh of the total n-layer grown, it is essential that both growth and assessment are performed accurately. A mere 3.5-percent error in the total n-layer width may constitute an error of approximately 25 percent

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in the relatively narrow active region width. The procedure for thickness assessment used is the jet etch and strain method [2] which delineates the n-n^+ interface, followed by an optical interference fringe method [3]. Measurement resolution of better than 500 Å representing approximately 1.5 percent of the total layer width is achieved.

The graded p^+-n junction is produced by depositing into the as-grown n-layer a shallow source of acceptor impurity atoms followed by a drive-in period at high temperature. The deposition has been effected both by thermal diffusion from oxidized boron nitride and by implantation of boron ions. The latter method is favored owing to the greater degree of control and reproducibility it affords. Early drive-in experiments using a pure inert gas environment were abandoned in favor of a 5-percent oxygen 95-percent inert gas (such as argon or nitrogen), as this gas mixture enhances the rate of diffusion of the boron atoms, leading to a reduction in the n-n^+ interface degradation. The drive-in, which lasts for approximately three hours and is performed at 1100°C, depletes the concentration of boron at the surface. This is replenished by a secondary low-temperature (860°C) diffusion of boron from an oxidized boron nitride source, resulting in low-resistance ohmic contacts without further effect on the rest of the impurity profile.

A sensitive check on the accuracy of the n-region width is the breakdown voltage of test diodes made from that material. For example, it has been empirically determined that optimum operation in the frequency range 8.5–9.5 GHz is achieved with devices with breakdown voltages between 28 and 34 V. Small adjustments to the drive-in time are sufficient to tailor the active region to the appropriate width. For operation in the frequency range 8–10 GHz, the complete material specification is as follows. A phosphorus-doped epitaxial layer, impurity concentration 7×10^{15} atoms/cm^3, thickness 3.6 μm, is grown onto an arsenic-doped substrate, impurity concentration 5×10^{19} atoms/cm^3. A dose of 5×10^{14} boron atoms/cm^2 is then implanted at 40 keV, to produce a peak concentration of 4×10^{19} atoms/cm^3. This is driven in for about three hours at 1100°C to produce an active region width of approximately 0.4 μm. The drive-in period also serves to anneal the implanted boron.

Finally, an 860°C, 30-min boron diffusion is effected to produce a 0.15 -μm p^+ contact layer. Fig. 1 illustrates the predicted final impurity doping profile.

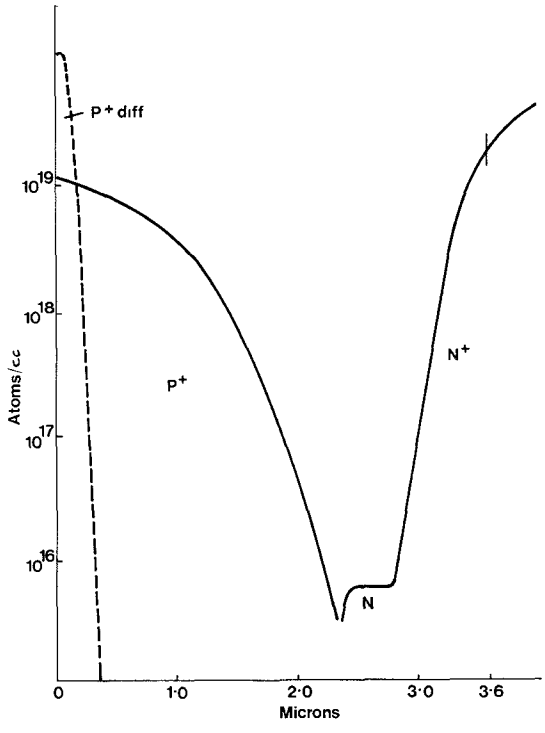


Fig. 1. *X*-band TRAPATT doping profile.

B. Device Thermal Design Considerations

Although the TRAPATT device has a relatively high efficiency, a substantial amount of dc power is dissipated as heat in the high field region. To maximize the dc power handling capability of the device and, hence, RF output, the junction must be provided with an efficient means of removing heat. TRAPATT's are generally operated in a pulse mode, thus both the mean and transient thermal response will determine the rate of change of temperature within the pulse, and also the maximum junction temperature at the end of each pulse, both of which limit the device RF performance and reliability. To minimize mean heating, integral-heat-sink (IHS) fabrication has been adopted. A high thermal conductivity metal is plated onto the device p^+ contact to provide a heat-sink as close as possible to the region of heat generation. The thermal impedance of the structure is reduced further by lapping the n^+ substrate to a minimum thickness, and then providing the n^+ contact with a second plated heat-sink [4] into which heat flows during the "on" time of the device. Heat flows in both directions from the junction during a pulse, providing the reservoir is close to the source of heat and with sufficient thermal capacity to act as a heat-sink. Heat flows from the reservoir through the device into the integral-heat-sink during the period between pulses. Choice of materials and dimensions for the two heat-sinks is determined by the pulse length, duty factor, and available fabrication technology.

C. Device Fabrication

The IHS fabrication procedure utilized in the production of TRAPATT diodes has been adopted from processes used in the production of high-frequency avalanche devices [5]. In order to minimize the thickness of silicon between the active region and the substrate contact (and, hence, minimize transient thermal impedance), an accurate substrate thinning process is adopted. The first stage in the fabrication process is to etch small diameter (approximately 50 -μm) holes into the p^+ side of

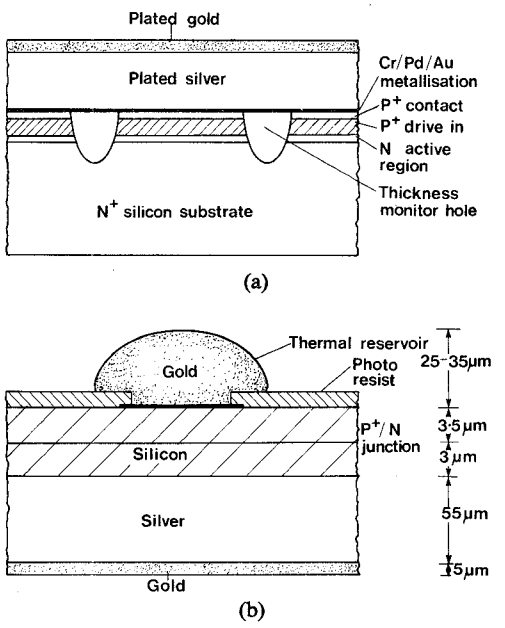


Fig. 2. (a) IHS TRAPATT fabrication process. (b) Final structure with thermal reservoir.

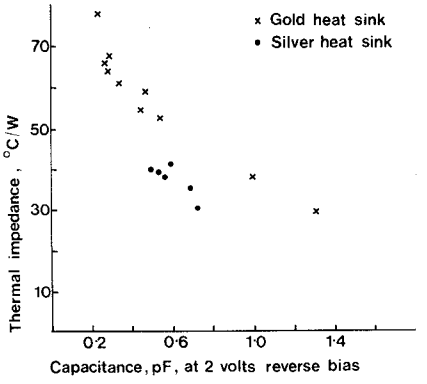


Fig. 3. A comparison between the CW thermal impedance of gold and silver heat sinks.

the wafer to a depth equal to the required final silicon thickness. A metal contact is made to this face by the sequential vapor deposition of chromium, palladium, and silver. Onto the silver layer is then deposited approximately 55 μm of electroplated silver followed by 5 μm of electroplated gold, Fig. 2(a). A reduction in CW thermal impedance of approximately 20 percent has been achieved with this heat sink compared with that of an all-gold system used in earlier work [3], Fig. 3.

The silicon substrate is thinned by lapping and polishing with successively finer grits until the thickness monitor holes appear. The total silicon thickness at this stage is approximately 7–8 μm. Contact is then made to the n^+ substrate by vapor deposition of chromium, palladium, and gold. Circular contact areas are defined on this metal contact and gold heat reservoirs plated onto the areas through holes in a thick (3–5-μm) photoresist layer. Mesa devices are then defined by etching the silicon through to the p^+ contact metallization. Finally, devices are separated by cutting through the metal heat-sink. Fig. 4(a) and (b) illustrate the completed device.

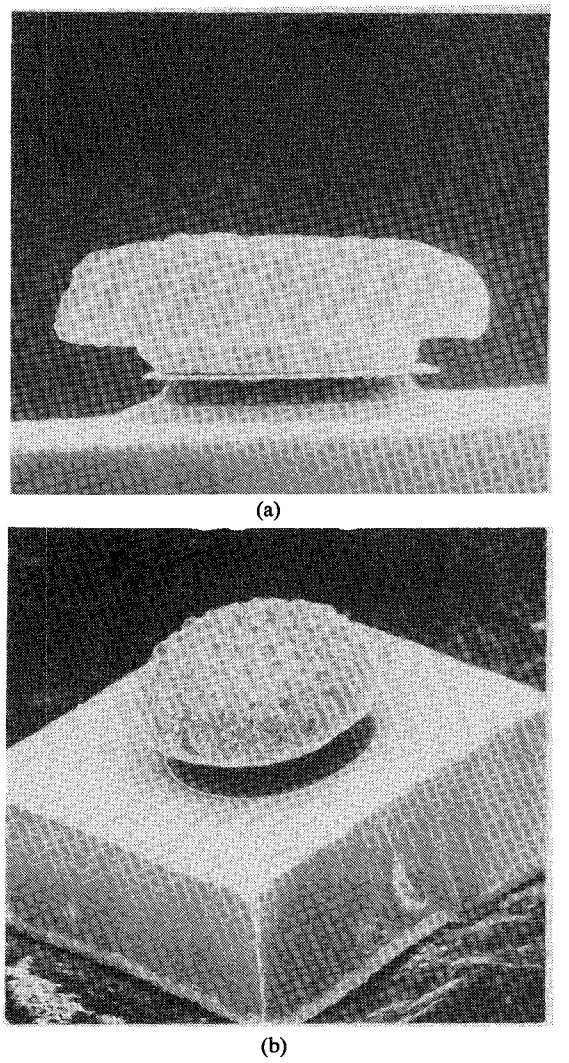


Fig. 4. (a) Completed TRAPATT diode. (b) Device with integral silver/gold heat sink.

D. Device Dimensional Design

The reverse-bias junction capacitances at breakdown of the TRAPATT diodes found to operate as oscillators or amplifiers in *I* band, lie in the range 0.25–1.20 pF, corresponding to junction areas from 0.3 to 0.8×10^{-4} cm^2. Minimum dimensions of the device integral-heat-sink are determined by the particular device junction area. If, for example, a device of junction area approximately 0.4×10^{-4} cm^2 is used, it has been found that a plated heat-sink 200-μm square comprising approximately 55-μm silver, 5-μm gold provides an adequately low steady-state thermal impedance when bonded into a suitable microwave package. Particular care must be taken in the choice of silver-plating solution and method of plating [6]. In order for the back-contact heat reservoir to be effective, it must have a large enough thermal mass for its temperature not to change appreciably during a pulse and it must be close

enough to the heat source to have effect during the pulse. From Fig. 2(b) it can be seen that the thermal paths to both integral-heat-sink and the thermal reservoir include approximately 3 μm of silicon with a thermal time constant of about 500 ns, consequently both plated regions are potentially effective heat-sinks for pulses in excess of half a microsecond duration. Plated reservoirs thicker than the 35 μm indicated in Fig. 3(b) do not significantly reduce the transient thermal impedance for 5-μs pulsewidths.

E. Device Packaging

Completed devices are ultrasonically bonded into AV162[1] microwave packages, the 5-μm gold-plated layer on the silver heat-sink being instrumental in obtaining good thermal intimacy between the device and package. A gold wire is then thermocompression-bonded to connect the device to the package rim.

III. Circuit Description

Stable fundamental frequency *X*-band TRAPATT reflection amplification has been obtained in both coaxial and microstrip circuits [3], [6], [8].

The TRAPATT amplifier circuit first investigated used a 50-Ω 3.5-mm diameter coaxial airline which supported a pure TEM mode to approximately 40 GHz [3]. A low-pass filter matching network was placed at less than the fundamental wavelength from the diode plane [9]. The circuit was very similar in configuration to that used in the time-domain-triggering (TDT) TRAPATT oscillator circuits described in the literature [10]. The appropriate matching network was realized by adjustment of three 20-Ω anodized aluminium slugs.

The diodes, as stated, were bonded in AV162 packages with high cutoff frequencies [11]. These circuits operated well giving gains of 7 dB with input signal levels of 1.2 W, and 3 dB with input signal levels of 5 W. Power-added efficiencies as high as 25 percent and bandwidths of 500 MHz were demonstrated [3]. However, this circuit tended to support spurious signals at frequencies corresponding to oscillator operation in the TDT mode. It was subsequently found that placing the filter network close to the diode package [12] eliminated these spurious signals.

This circuit arrangement also minimized the cavity slope reactance $dX/d\omega$, a necessary requirement for obtaining wide bandwidths, and enabled the efficient operation of larger area TRAPATT diodes. Provided the amplified signal was free from noise and pulse breakup, measurements over the frequency range of 2–18 GHz demonstrated that any spurious signals were 30–40 dB below the amplified signal.

The amplifier circuit contained a smaller number of matching sections than the conventional TRAPATT oscillator circuits [3]. The impedances and positions of the matching sections were empirically derived. The circuit consisted of a 50-Ω 3.5-mm diameter coaxial line, with the packaged diode mounted at the end of the line. A single low impedance 20-Ω section was placed close to the diode package, followed by a second, usually shorter, 20-Ω section. A pair of (TEFLON) inner supports were placed between the filter section and the bias network; these had a considerable influence upon bandwidth and the minimum signal level required to trigger the amplifier circuit. Variations in the circuit and package-bonding configurations were found necessary, depending upon the size of the diode to be matched. For example, a small area, 0.3×10^{-2}, diode of breakdown capacitance 0.25–0.35 pF required a high-inductance bonding configuration, a single 0.0012-cm diameter gold wire between the chip and the package, and a small PTFE slug 1.0 mm in length between the packaged diode and the first low impedance section of the matching network. Whereas larger area 0.8×10^{-4}-cm^2 devices of breakdown capacitance 0.6–1.3 pF required the first impedance matching section to be closer to the diode package and a lower inductance gold wire of diameter 0.0025 cm bonded between package and chip.

The operation of the amplifier using the circuit configuration described is not fully understood, as it precludes the classical TDT mechanism which is encountered in the TRAPATT oscillator. Mackintosh [13], [14] has described a simple theoretical circuit model for a TRAPATT oscillator which was not dependent upon the classical TDT mechanism. The model may go some way to explaining the operation of the TRAPATT amplifier, and is consistent with the wide negative resistance bandwidths observed. *I*-band TRAPATT amplifiers operating with pulses of the order of 0.5 μs and duty factors of 1 percent have shown 3-dB gain bandwidths of greater than 11 percent with maximum gain of 5 dB. The usable bandwidth was smaller, as there were regions of noisy operation where the device was no longer optimally matched.

A. Biasing Techniques

The TRAPATT amplifiers were operated in class C [15] by biasing the diode below its breakdown voltage. In this state, the diode was in effect switched-off, and negligible current flowed through it. When an RF signal of sufficient amplitude was applied, the TRAPATT mode was triggered, the voltage dropped below the bias voltage, a large current flowed through the diode, and RF amplification occurred. In the absence of the RF signal, the diode returned to its off-state, with negligible current flow. Biasing was applied by a dc voltage just below the breakdown voltage of the diode. A resistance–capacitance network in the biasline absorbed the diode voltage dropback, as the diode switched into the TRAPATT mode and suppressed ringing in the bias circuit. Small area diodes, 0.3×10^{-4}cm^2, with breakdown capacitances of the order of 0.3 pF, and operating at a current level of 300–400 mA, required a bias load resistance of approximately 12 Ω. Larger area diodes 0.8×10^{-4}cm^2 with breakdown capacitances of 1 pF, operating at a current level of greater than 1 A, required a bias load resistance of 2–4 Ω. In practice it

[1]Interceram, Inc.

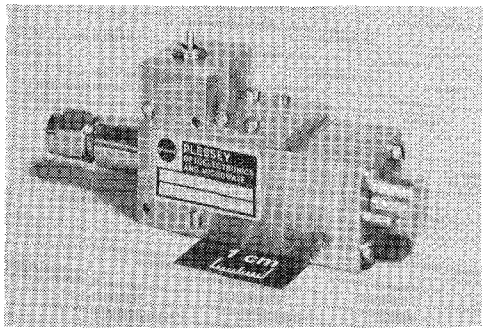
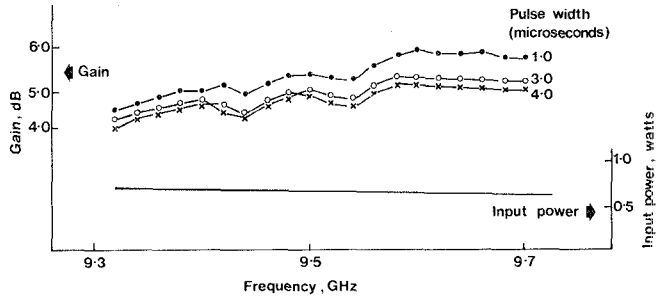
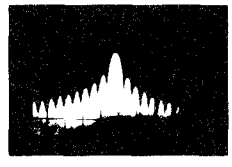


Fig. 5. Rugged TRAPATT amplifier cavity.



(a)



(b)

Fig. 6. (a) TRAPATT amplifier with varying input pulsewidth. (b) Amplified 4-μs pulse spectrum.

was found to be important to operate at the correct dc load-line point, otherwise noisy and unstable operation was obtained, often accompanied by limited bandwidth and poor RF rise-time. Voltage spikes on the average voltage switching waveform could be suppressed by including ferrite beads in the bias circuit line, these helped to reduce spike-induced burnout, with little degradation in RF rise-time, this being typically 40–60 ns for a single-stage TRAPATT amplifier.

B. Ruggedized Coaxial Circuit

To fulfill systems requirements of tolerance to vibration and shock, a novel, rugged TRAPATT cavity with internal biasing (Fig. 5) was developed. The cavity consisted of a number of metal plates of various thicknesses which were mounted together to reproduce the characteristics of the slug-tuned cavity. Shims were used to adjust the relative positions of the matching sections, so providing fine tuning. The plates were located by dowels and could be clamped firmly together to produce a rugged TRAPATT amplifier circuit. The cavity could withstand a vibration of 23-g rms over a spectrum of 10–2000 Hz, without a measurable degradation of the microwave performance.

IV. Microwave Performance

The TRAPATT amplifiers have been operated with power-added efficiencies as high as 25 percent in *I* band [3], whereas *I*-band TRAPATT oscillators have given efficiencies in excess of 35 percent [16], [17].

The TRAPATT amplifier requires a minimum input signal level before amplification is initiated. The threshold input signal level depends upon the area of the device, small area devices requiring levels of the order of 0.5 W, and larger area devices 1–3 W. With increasing signal drive level, the gain characteristic is linear at 3–7 dB, before going into saturation and finally compression. The TRAPATT device is essentially suited to large-signal low-gain applications.

To obtain the most effective power budget in cascaded amplifier design, it is necessary to use small area devices in the initial stages and larger area diodes in the output stages. Small area diodes, corresponding to breakdown capacitance 0.25–0.35 pF, allow the operation of efficient TRAPATT reflection amplifiers with an input signal drive level of 500–700 mW. At pulsewidths of 1 μs and duty factors of 1 percent, gains greater than 6 dB with 1-dB bandwidths in excess of 400 MHz at a center frequency of approximately 9.4 GHz have been obtained at maximum power-added efficiency of approximately 16 percent. Gains of 8 dB with power-added efficiencies in excess of 18 percent have been obtained over narrower 1-dB bandwidths, 170 MHz, again centered at approximately 9.4 GHz. For many systems applications it is necessary that the device operates over long pulsewidths. Fig. 6(a) shows the operation of a TRAPATT amplifier with an input of approximately 600 mW and pulsewidths between 1 and 4 μs making use of the improved thermal structure as discribed earlier. Fig. 6(b) shows the frequency spectrum for an amplified 4-μs pulsewidth. Devices have been operated with pulselengths of greater than 8 μs with gains of 4 dB over 1-dB bandwidths of 400 MHz centered at 9.3 GHz. For long pulsewidth operation, it was experimentally determined that devices with low leakage currents of the order of 100 nA were less prone to tuning induced burnout.

The S_{11} parameters at the diode package plane for both amplifier and oscillator circuits have been measured between 8 and 12 GHz using an HP network analyzer. The measurements indicated that the amplifier circuit impedance at the fundamental frequency had a real component of 10–20 Ω, compared with 5–8 Ω for the oscillator. The impedances suggest that larger area diodes should be more readily matched as amplifiers, and this has been experimentally verified. Fig. 7 shows that the added-power efficiency of an amplifier decreases with increasing device breakdown capacitance, whereas the oscillator shows a linear decrease in efficiency with device breakdown capacitance.

For large input signal levels of 3.6 W over 0.5-μs pulsewidth with a 1-percent duty factor, Fig. 8 shows the bandwidths obtained for a range of diodes with breakdown capacitances between 0.94 and 1.2 pF. The added power efficiency was as high as 20 percent with gains of about 3 dB.

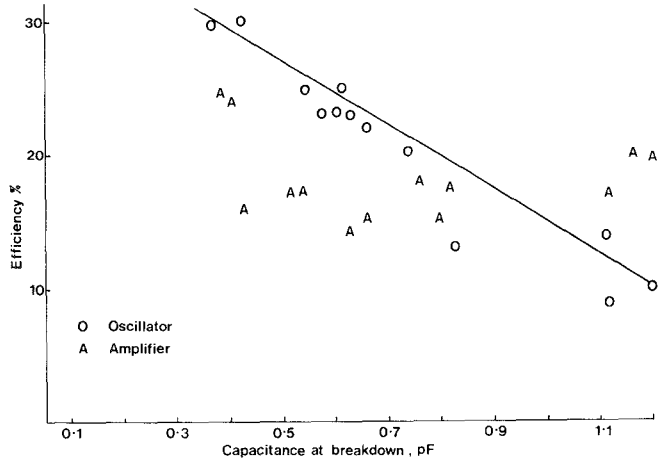


Fig. 7. Efficiency of amplifier and oscillator versus diode breakdown capacitance.

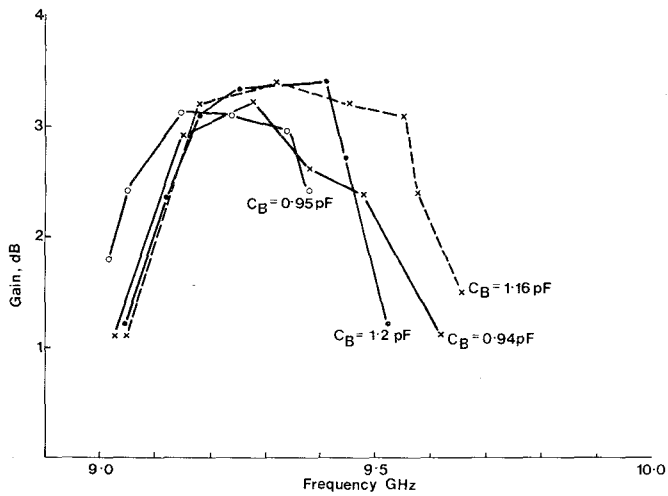


Fig. 8. Large input signal amplification.

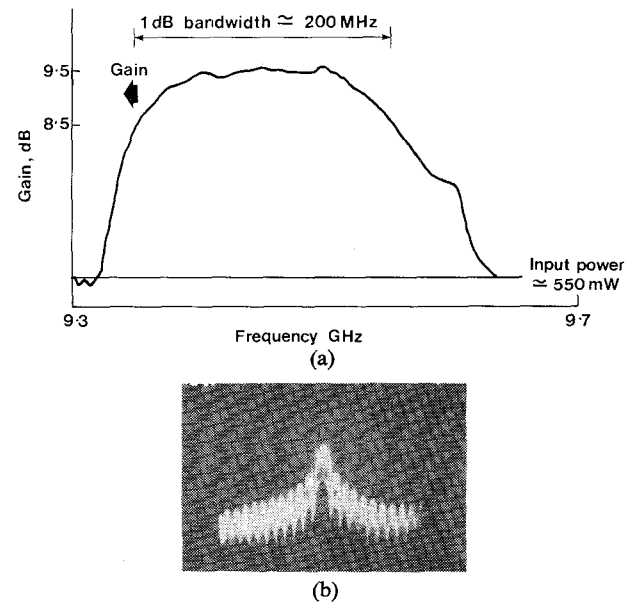


Fig. 9. (a) Cascaded TRAPATT amplifier gain response. (b) Amplified 1-μs pulse spectrum.

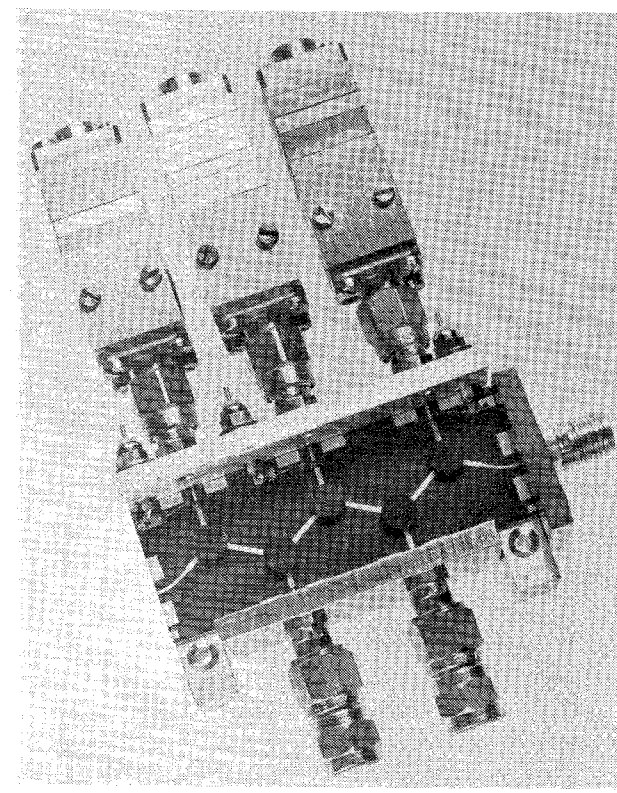


Fig. 10. Three-stage TRAPATT amplifier assembled using microstrip circulators and isocirculators.

A. Cascaded TRAPATT *Amplifiers*

To increase the gain and peak power of the amplifier, TRAPATT class-C reflection amplifiers have been cascaded. Fig. 9(a) shows the gain-frequency response of a two-stage cascaded TRAPATT amplifier constructed with SMA coaxial circulators. The first stage contained a diode of breakdown capacitance of approximately 0.3 pF, and the second stage used a larger area device with a breakdown capacitance of 0.6 pF. With an input signal of 550–700 mW, a pulsewidth of 1 μs, and a 1-percent duty factor, an overall gain of 9.5 dB was realized. Fig. 9(b) shows the amplified 1-μs pulse spectrum. Isolation between the stages was found to be necessary to reduce noisy operation. The amplifier operated in the class-C mode from dc supply rails and used a capacitance–resistance load line as previously described. The feasibility of this unit being driven by an FET driver stage was demonstrated. The overall gain of the complete unit including the FET driver stage was 26 dB, with a maximum output power of 4.6 W and a 1-dB bandwidth in excess of 200 MHz at a center frequency of 9.4 GHz.

By utilizing integrated microstrip circulators and isocirculators, and coupling miniature TRAPATT cavities via OSM launchers to the microstrip circuit, a complete three-stage TRAPATT amplifier was assembled and is shown in Fig. 10. Both thick and thin film techniques were used to fabricate circulators, isocirculators [19], bias filters, and dc blocks on a single 5.08×2.54-cm ferrite substrate. The microstrip circuit was assembled in a box lined with lossy material so as to reduce box-made resonances. The TRAPATT cavities were a miniaturized form of the 3.5-mm diameter 50-Ω coaxial ruggedized circuit already described. The unit gave a gain of 9–10 dB with

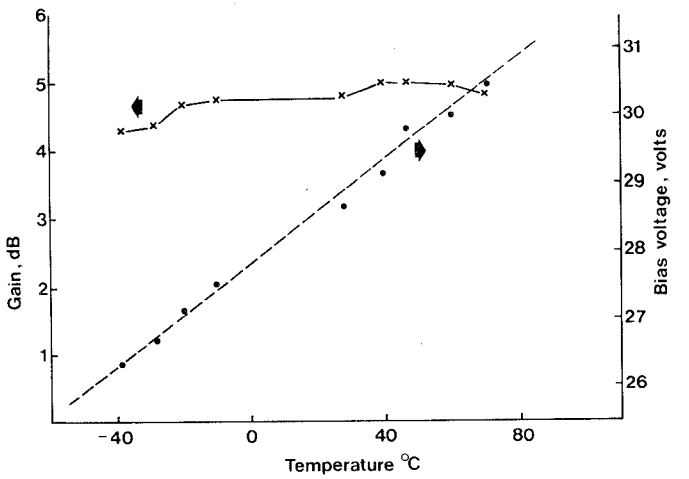


Fig. 11. Operation of TRAPATT amplifier over a temperature range.

an output peak power in excess of 10 W, with an overall added power efficiency of approximately 7 percent for pulsewidths between 0.5 and 1.0 μs at a center frequency of 9.7 GHz. The cascaded TRAPATT amplifiers showed a degradation in RF rise-times and an increase in switch-on delay.

Cascaded TRAPATT pulsed, class-C amplifiers have been demonstrated, but difficulties were experienced in obtaining an added power from each successive amplifier stage. The problem was thought to be a result of having poor harmonic isolation between stages. The isolation between stages was measured as greater than 50 dB at the fundamental frequency of 9.7 GHz, but would be relatively poor at the harmonics. Consequently, each successive TRAPATT stage provided a harmonic mismatch to the preceeding TRAPATT stage, causing noisy and low gain operation. However, by adjusting the line lengths between stages, some degree of tuning could be effected enabling successful operation of multiple cascaded reflection TRAPATT amplifiers.

As with the majority of solid-state devices, the TRAPATT requires subsidiary electronic circuitry to provide protection, temperature compensation, and correction of intrapulse phase shift with increasing pulsewidth, in order to maximize the versatility of the amplifier. These circuit techniques are described below.

B. Temperature Performance

A large-signal amplifier giving a maximum gain of 5 dB at a center frequency of 9.5 GHz has been operated over a temperature range of -40–70°C, with a maximum variation in gain of 0.75 dB. This was obtained by linearly increasing the bias voltage by approximately 12 percent with increasing temperature (Fig. 11).

C. Intrapulse Phase Variation

The TRAPATT diode junction temperature rises rapidly with increased pulse lengths causing transient impedance changes with consequent droop in gain across the pulsewidth of the amplified signal and a reduction in the overall efficiency of the amplifier. It was experimentally

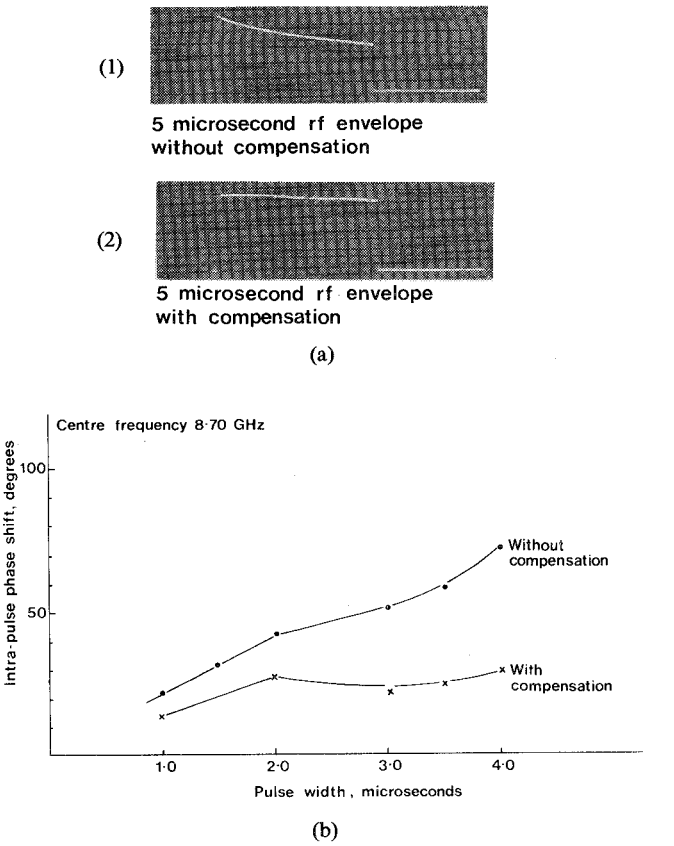


Fig. 12. (a) A comparison between an amplified 5-μs RF envelope without and with electronic compensation. (b) Intrapulse phase of a single stage TRAPATT amplifier.

observed that there was approximately a linear increase in intrapulse phase shift as the amplified pulse was lengthened. For a single-stage TRAPATT amplifier, an amplified 4-μs pulsewidth resulted in a total intrapulse phase shift of 100°. Both gain reduction and intrapulse phase shift are undesirable in pulse compression radars and many other systems applications.

A simple method of minimizing both gain droop and intrapulse phase shift with increasing pulsewidth was developed for the class-C TRAPATT amplifier. This consisted of an electronic compensation circuit which derived its trigger from the voltage drop-back which resulted across the TRAPATT diode when an RF input signal was applied to the amplifier. The trigger circuit switched off with the voltage recovery, on removal of the RF input signal. The trigger signal was, therefore, approximately the length of any input signal applied to the amplifier and was used to initiate a variable exponential current source. This was superimposed upon the current being drawn from the constant voltage supply, thus shaping the current waveform to the TRAPATT device. Significant improvements in both gain and intrapulse phase were observed. Fig. 12(a) shows a comparison between an amplified 5-μs RF envelope from both an uncompensated and a compensated TRAPATT amplifier. An improvement in gain of 12–20 percent for a single stage TRAPATT amplifier could be realized, and it was also noted that there was an improvement in bandwidth for long pulsewidth operation. Without compensation, a 4-μs amplified pulse showed a

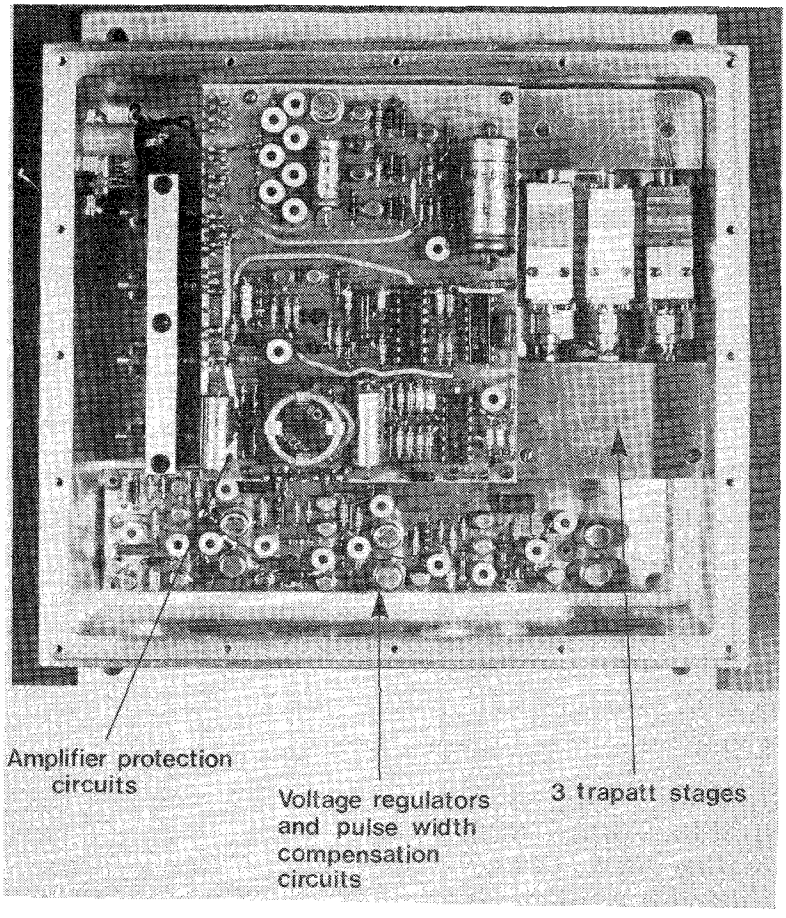


Fig. 13. Three-stage class-C TRAPATT amplifier with protection and pulse compensation circuitry.

3-dB bandwidth of approximately 270 MHz, whereas with compensation the identical amplifier showed a 3-dB bandwidth of greater than 400 MHz. Fig. 12(b) demonstrates significant improvements in intrapulse phase across the pulse; for a 4-μs pulsewidth the phase shift was greater than 70°, whereas with compensation this was reduced to less than 30°. Obviously, further improvements could be obtained if the relationship between temperature and pulsewidth were determined and exactly compensated for, rather than the first-order approximation adopted.

Fig. 13 shows a completed 10-W TRAPATT amplifier. It consisted of three TRAPATT reflection amplifier stages linked together by microstrip circulators and isocirculators as described. The complete unit was supplied from a single 36-V rail, and the voltage to each TRAPATT stage was controlled by voltage regulators, allowing the appropriate breakdown voltage to be set for each diode. The amplifier stages were electronically compensated, to regulate both gain and intrapulse phase variations with pulsewidth. To protect the TRAPATT diodes and electronic circuitry, a current limit and an excess voltage switch were included. To afford protection against a quasi-CW input signal, an input pulsewidth limiting circuit was added. This circuit compared the length of pulse derived from the voltage drop-back across the TRAPATT diode with a predetermined value, which could be set in the range from 1 to 10 μs. If this value were exceeded, then the supply rail to the TRAPATT amplifiers was electronically switched off in approximately 500 ns.

D. Efficiency of Overall Unit

Despite the high intrinsic efficiency of each TRAPATT device, the efficiency of the basic three-stage cascaded amplifier was reduced to approximately 7 percent when the losses and compromises in the microwave circuit were included. Addition of the electronic circuitry with its inherent loss further reduced the efficiency significantly. This is typical of the degradation that occurs from a laboratory state-of-the-art unit to a system prototye.

V. Conclusions

The development of silicon TRAPATT diodes and improved circuit techniques has resulted in the demonstration of efficient *I*-band TRAPATT pulsed amplifiers. The successful operation of the TRAPATT device with power FET driver stages, microstrip technology, and electronic circuitry for the correction of intrapulse phase deviation, demonstrated that the TRAPATT, like other solid-state devices, can be integrated into relatively complex subsystems.

Cascading reflection TRAPATT amplifiers has been shown to be feasible, but difficulties were experienced in obtaining the expected added powers and gains, which

consequently led to an overall efficiency of approximately 7 percent for a three-stage amplifier.

The *I*-band TRAPATT oscillator results of 15 W with 36-percent conversion efficiency are comparable with the state-of-the-art short-pulse (500-ns) operation of modified-Read-profile GaAs IMPATT's (16.8 W at 9.3 GHz at 32 percent). However, the inherently thinner active region width (0.3 μm versus approximately 2.5 μm) enables the TRAPATT to be operated over greater pulsewidths. The diodes described in this paper suffered a thermal penalty of about 3 μm of p^+ contact material. It is anticipated however, that attention to reduction of the contact region width would enable operation to be extended from the present limit of about 7 μs to periods in excess of 20 μs with a corresponding increase in mean operating levels. The complexity of circuit matching requirements probably limits fundamental TRAPATT operation to about 12 GHz, though the potential of harmonic extraction remains to be determined.

As an amplifier, the TRAPATT's unique voltage "cutback" characteristic enables operation in a class-C mode to be readily achieved. Alternative high-efficiency amplifiers may exhibit comparable performance over the operating pulse; however, their mean efficiency would be small in low duty-cycle operation. TRAPATT operation in class C permits overall efficiencies in excess of 20 percent to be realized for a range of duty factors and pulsewidths making the device suitable for ECM applications.

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